In the Claims

1.-32. (canceled)

33. (previously presented)A method used to form a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly having a planarized wafer surface and at least first and second features in spaced relation to each other which define a region comprising an opening between said first and second features;

forming a conductive layer over said first and second features and within said opening;

providing a patterned mask layer over said conductive layer, said patterned mask layer having an opening therein which exposes said region between said first and second features;

etching said conductive layer within said opening between said first and second features using a continuous etch comprising:

a first etch which erodes said conductive layer with ions traveling in a first direction substantially perpendicular with a plane of said planarized wafer surface and leaves conductive stringers between said first and second features subsequent to said first etch; then

a second etch which electrically charges said ions to bend said charged ions into said stringers in a second direction which is less perpendicular with said plane of said planarized wafer surface than said first direction and removes said conductive stringers remaining between said first and second features.

34.-36. (canceled)

37. (previously presented) A method used to form an electronic device having a semiconductor device, the semiconductor device formed by a method comprising:

providing a semiconductor wafer substrate assembly having a planarized wafer surface and at least first and second features in spaced relation to each other which define a region comprising an opening between said first and second features;

forming a conductive layer over said first and second features and within said opening;

providing a patterned mask layer over said conductive layer, said patterned mask layer having an opening therein which exposes said region between said first and second features;

etching said conductive layer within said opening between said first and second features using a continuous etch comprising:

a first etch which erodes said conductive layer with ions traveling in a first direction substantially perpendicular with a plane of said planarized wafer surface and leaves conductive stringers between said first and second features subsequent to said first etch; then

a second etch which electrically charges said ions to bend said charged ions into said stringers in a second direction which is less perpendicular with said plane of said planarized wafer surface than said first direction and removes said conductive stringers remaining between said first and second features.

38. (previously presented)The method of claim 37 further comprising:

during said first etch:

introducing an oxygen-containing gas into a chamber at an oxygen flow rate of between about 1.9 sccm and about 2.7 sccm;

introducing a halogen-containing gas into said etch chamber at a halogen flow rate of between about 35 sccm to about 65 sccm; and

subjecting said semiconductor wafer substrate assembly to a top power of between about 245 watts to about 315 watts; and

during said second etch:

increasing said flow rate of said oxygen-containing gas to an oxygen flow rate of between about 3.6 sccm to about 4.7 sccm;

maintaining said halogen-containing gas flow rate at a halogen flow rate of between about 35 sccm to about 65 sccm; and

increasing said top power to between about 385 watts and about 455 watts.

39. (new) The method of claim 33 further comprising forming a polysilicon layer during said formation of said conductive layer over said first and second features and within said opening.

40. (new) The method of claim 39, further comprising:

during said etch of said conductive layer with said first etch, etching said polysilicon with an etch comprising a flow rate of between about 1.9 sccm and 2.7 sccm of an oxygen-containing gas, a flow rate of between about 35 sccm to about 65 sccm of a halogen-containing gas, and a top power of between about 245 watts and about 315 watts; and

during said etch of said conductive layer with said second etch, etching said polysilicon with an etch comprising a flow rate of between about 3.6 sccm and about 4.7 sccm of an oxygen-containing gas, a flow rate of between about 35 sccm to about 65 sccm of a halogen-containing gas, and a top power of between about 385 watts to about 455 watts.

41. (new) The method of claim 39, further comprising:

during said etch of said conductive layer with said first etch, etching said polysilicon with an etch comprising an oxygen flow rate of between about 1.9 sccm and 2.7 sccm, a flow rate of about 55 sccm of a halogen-containing gas, and a top power of between about 245 watts and about 315 watts; and

during said etch of said conductive layer with said second etch, etching said polysilicon with an etch comprising an oxygen flow rate of between about 3.6 sccm and about 4.7 sccm, a flow rate of about 55 sccm of a halogen-containing gas, and a top power of between about 385 watts to about 455 watts.

42. (new) The method of claim 37 further comprising forming a polysilicon layer during said formation of said conductive layer over said first and second features and within said opening.

43. (new) The method of claim 42, further comprising:

during said etch of said conductive layer with said first etch, etching said polysilicon with an etch comprising a flow rate of between about 1.9 sccm and 2.7 sccm of an oxygen-containing gas, a flow rate of between about 35 sccm to about 65 sccm of a halogen-containing gas, and a top power of between about 245 watts and about 315 watts; and

during said etch of said conductive layer with said second etch, etching said polysilicon with an etch comprising a flow rate of between about 3.6 sccm and about 4.7 sccm of an oxygen-containing gas, a flow rate of between about 35 sccm to about 65 sccm of a halogen-containing gas, and a top power of between about 385 watts to about 455 watts.